I. Listing of Claims

1. (Previously Presented): An integrated field-effect transistor, having a substrate region surrounded:

by two terminal regions, one terminal region being a source region and the other terminal region being a drain region, the source region being arranged at a first side of the substrate region and the drain region being arranged at a second side of the substrate region, the first and second sides being opposite sides of the substrate region;

by two electrically insulating insulating layers, which are arranged at a third and fourth side of the substrate region, the third and fourth sides being mutually opposite sides of the substrate region and the insulating layers being adjoined by control regions, the control regions being located along the third and fourth sides with an insulating layer of the insulating layers between each of the control regions and the substrate region, the first and second sides being narrower than the third and fourth sides;

by two electrically insulating regions, the insulating regions being arranged at mutually opposite sides of the substrate region, a first insulating region of the insulating regions being arranged at a fifth side of the substrate region and a second insulating region of the insulating regions being arranged at a sixth side of the substrate region, and

by an electrically conductive connecting region or a part of an electrically conductive connecting region which produces an electrically conductive connection between one of the terminal regions and the substrate region, the connecting region comprising a metal-semiconductor compound,

part of a covered area of the substrate region being covered by the connecting region, the connecting region also covering a covered area of the source region such that the connecting region extends across the first side of the substrate region to the source region, the part of the covered area of the substrate region being located between the insulating layers and between the control regions.

2. (Original): The field-effect transistor as claimed in claim 1, wherein the conductive connecting region comprises at least one of: a silicide of a metal having a melting point of greater than 1400 degrees Celsius, a refractory metal silicide or a rare earth metal silicide.

3. (Original): The field-effect transistor as claimed in claim 1, wherein at least one of:

the insulating layers for insulating the control regions from the substrate region have an insulation strength of at least fifteen nanometers,

a distance between the terminal regions is at least 0.3 micrometer, and

one terminal region or both terminal regions have a shallow doping profile gradient which permits a switching voltage having a magnitude of greater than five volts.

4. (Original): The field-effect transistor as claimed in claim 1, wherein at least one of:

one insulating region is part of an insulating layer which carries a multiplicity of field-effect transistors,

the insulating layer comprises silicon dioxide, and

the other insulating region is part of an insulating layer, which insulates a multiplicity of substrate regions.

5. (Previously Presented): The field-effect transistor as claimed in claim 1,

wherein the substrate region at least one of:

contains a monocrystalline semiconductor material; and

is doped in accordance with one conduction type and the terminal regions are doped in accordance with another conduction type.

6. (Original): The field-effect transistor as claimed in claim 1, wherein the control regions are electrically conductively connected to one another.

7. (Original): The field-effect transistor as claimed in claim 1, wherein at least one of:

the substrate region contains six side areas,

the terminal regions are arranged at mutually opposite sides of the substrate region, and

the control regions are arranged at mutually opposite sides of the substrate region.

8. (Original): The field-effect transistor as claimed in claim 1, wherein switching voltages having a magnitude of greater than nine volts are able to be switched by the field-effect transistor.

9. (Original): The field-effect transistor as claimed in claim 1, the field-effect transistor being a driving transistor on a word line or a bit line of a memory cell array, the driving transistor applying a control voltage to the word line or to the bit line.

10-14. (Cancelled).

15. (Previously Presented): The field effect transistor as claimed in claim 1, wherein the substrate region is p-doped.

16. (Previously Presented): The field effect transistor as claimed in claim 1, wherein the substrate region is n-doped, thereby producing a p-channel enhancement mode transistor.

17. (Cancelled).